28.6 1.83ps-Resolution CMOS Dynamic Arbitrary Timing Generator for >4GHz ATE Applications

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The operating frequencies of LSIs have reached the GHz range. For testing such high-speed devices, automatic test equipment (ATE) must have a timing accuracy on the order of ps with flexible timing control and a high-speed test rate above GHz. In order to realize a high-speed and high-precision timing generator (TG) for ATE, the use of GaAs [1] or bipolar technology is effective. However, such an approach causes an increase in hardware cost, size and power consumption.

CMOS technology is excellent for high integration, low power consumption, and low cost. However, it has been very difficult to realize a high-speed, high-precision TG using CMOS circuitry because of large switching noise and rapid fluctuations in temperature due to a change in circuit activity. A previously reported CMOS TG achieved an operating frequency of 100 to 400MHz, a resolution of 19.5ps, and an integral non-linearity (INL) of 35ps [2]. This TG required thousands of SRAM macros to store calibration data for a timing vernier. However, the use of calibration-RAMs causes an increase in chip size. More address/data bits of RAM are required to achieve finer resolution. A 100× increase in the size of the calibration RAM would be required to achieve a resolution of several ps. Moreover, the access time required for the calibration RAM would limit the operating frequency of the TG.

This paper describes a high-speed, high-precision fully CMOS dynamic arbitrary timing generator for >4GHz ATE applications. Maximum operating frequencies of 1.066GHz and 4.266GHz (when multiplexed), timing resolution of 1.83ps, INL less than ±4ps without a calibration RAM, and random jitter less than 0.7ps rms are achieved. These results are achieved by using the following techniques:
(1) A PLL/DLL multiple feedback system compensates thermal/voltage variation over the entire TG chip.
(2) A newly developed local-digital-DLL circuit generates precise delay, manages switching noise, and stabilizes self-heating to reduce timing jitter and drift.
(3) Reduced-swing signaling intra-chip interconnection improves operating frequency.
(4) A hysteresis-free phase detector drastically improves dead band and ripple jitter in a digital DLL.
(5) A high-linearity fine delay circuit achieves INL less than ±4ps without a calibration RAM.
(6) An active noise canceller suppresses switching noise and rapid changes in temperature in the TG.

Figure 28.6.1 is a simplified block diagram of our dynamic arbitrary timing generator, which includes a delay-control logic circuit and a timing vernier circuit. A 1.066GHz reference clock is used as a timing reference. A coarse delay value, with a resolution equal to the period of the reference clock, is obtained by counting the clock and retrieving the required edges using the delay-control logic circuit. A fine delay value, with resolution finer than the period of the reference clock, is then added by the timing vernier circuit. The delay setting can be dynamically changed on-the-fly to provide a flexible timing setting cycle by cycle. Because of this dynamic operation, circuit activity can change drastically during a short period of time, causing rapid fluctuations in the chip temperature and supply voltage due to *IR* drops inside and outside the chip.

To eliminate timing drift and jitter due to such rapid changes in temperature and voltage, a PLL/DLL multiple feedback system is utilized. The PLL feedback system compensates slow variations in the temperature and voltage of the entire chip due to the average variation of circuit activity on the chip. The DLL feedback system compensates faster variations in the local temperature and voltage in each timing vernier block.

This local-DLL circuit functions as a 16-phase clock generator, and it performs as a precise timing vernier with a 16:1 multiplexer (MUX) and low-INL fine delay. A DLL-based timing vernier has advantages such as stability, accuracy, and low-noise performance because of its constant circuit activity. These advantages can eliminate the need to use a calibration RAM [3]. This local-DLL circuit has a digital feedback system and no large analog filters, and its layout area is very small. In order to minimize size and power dissipation, one local-digital-DLL is shared by eight timing vernier circuits. An exemplary chip has five local-digital-DLL blocks and 40 1.066GHz timing outputs. To achieve 1.066GHz operation, reduced-swing signaling is used for critical paths such as clock distribution and the multiplexer for the 16-phase clock.

In digital-DLL circuits, ripple jitter due to a dead-band in the phase detector can be problematic. Figure 28.6.2 shows an ordinary static flip-flop (FF) in a phase detector that has a dead-band due to of the hysteretic transfer characteristic caused by its positive-feedback circuitry (a). This causes large ripple jitter. We used a pre-sampling technique using a dynamic FF (b) that has no positive feedback. Less than ±1.5ps of dead-band and less than ±2.5ps of ripple jitter are achieved.

It is impossible to achieve monotonicity in an ordinary multi-stage fine-delay circuit with switching delay buffers. For this reason the use of a calibration RAM is required [2]. We developed a 1-stage current-controlled high-linearity fine-delay circuit shown in Fig. 28.6.3. This circuit achieves a delay resolution of 1.83ps, INL less than $3ps_{pp}$ without a calibration RAM, and a delay span of 58.6ps, which is needed for interpolation for 16-phase clocks. The delay-versus-bias-current characteristic is a hyperbola and the delay span (gain) can be adjusted by offset bias. Less than 300ps of settling time for changing the delay setting is also achieved.

The local-digital-DLL circuit is always active, so it does not cause any I_{DD}/I_{SS} fluctuation. However, the I_{DD}/I_{SS} currents of the 16:1 MUX and the fine-delay circuit vary according to circuit activity. To eliminate those I_{DD}/I_{SS} fluctuations, we developed the active noise canceller shown in Fig. 28.6.4. This circuit generates a current that is the opposite of the fluctuation in I_{DD}/I_{SS} of the MUX and fine delay circuit, so the I_{DD}/I_{SS} current noise is eliminated.

A prototype chip was fabricated using a 0.18μm CMOS, Al 7-layer metal process. It has 40 circuits consisting of a 1.066GHz arbitrary timing generator and formatter, fail processing, real-time timing measurement function and many other features for test and measurement. The die aria is 14mm×14mm and the area of one local-digital-DLL block including eight 1.066GHz timing vernier circuits is 1.38mm×1.76mm. Output waveforms of the prototype TG chip generating 32ps, 4ps, and 1.83ps step delays and INL measurement results are shown in Fig. 28.6.5. The chip specifications and micrograph are shown in Figures 28.6.6 and 28.6.7 respectively.

References:
[1] A.Ohta et al., "A 12-ps-Resolution Digital Variable-Delay Macro Cell on GaAs 100K-Gates Gate Array Using a Meshed Air Bridge Structure," *IEEE J. Solid-State Circuits*, vol.34, pp. 33-41, Jan., 1999.
[2] B. Arkin, "Realizing a Production ATE Custom Processor and Timing IC Containing 400 Independent Low-Power and High-Linearity Timing Verniers," *IEEE ISSCC Dig. Tech. Papers*, pp.348-349, Feb., 2004.
[3] T. Okayasu, U.S. Patent 5491673, Feb., 1996.

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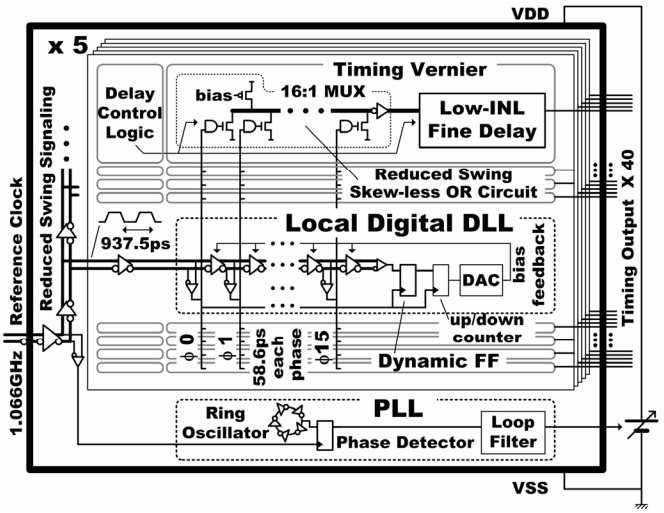

Figure 28.6.1: Dynamic arbitrary timing generator block diagram.

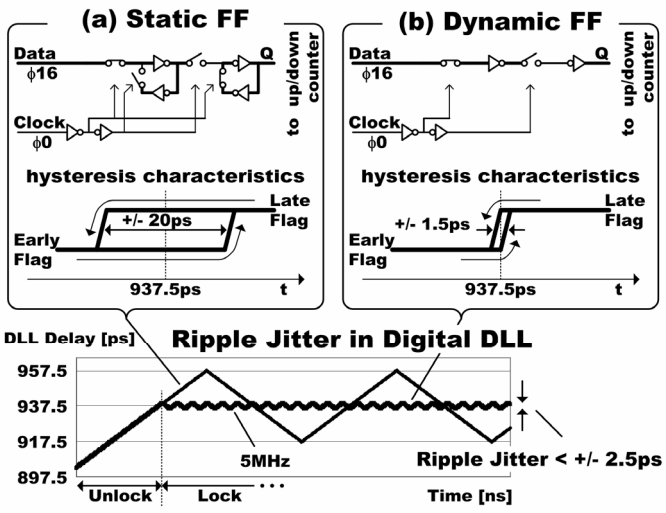

Figure 28.6.2: Ripple jitter improvement.

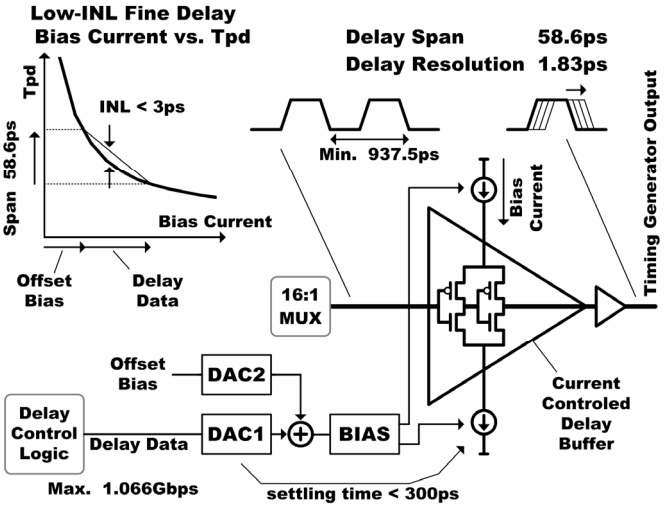

Figure 28.6.3: Low-INL fine delay.

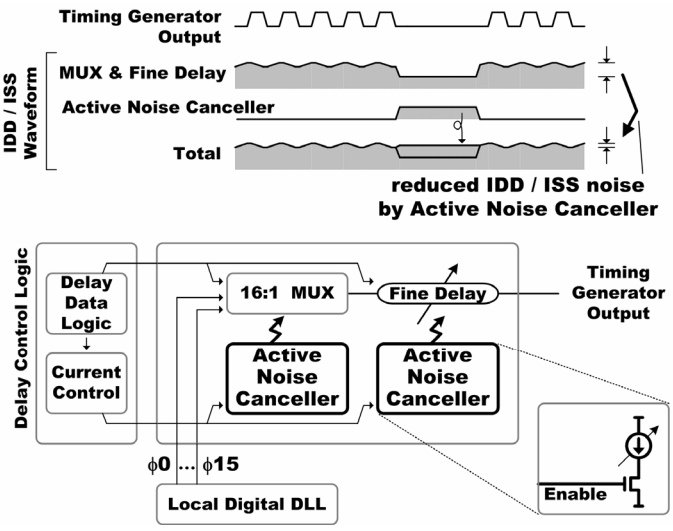

Figure 28.6.4: Active noise canceller.

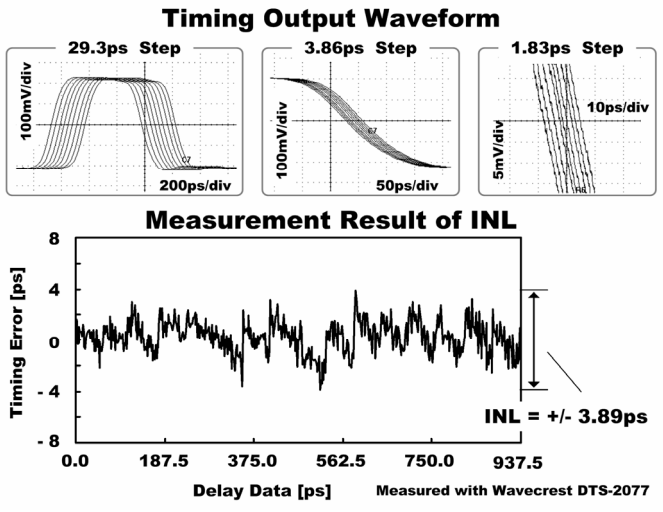

Figure 28.6.5: Measurement result.

Process	0.18 μm CMOS, Al 7-layer Metal
Chip Size	14.0mm x 14.0mm
# of Pins	625 pin FlipChip
Supply Voltage	2.5V and 1.8V
Power Dissipation	20.7W
# of Timing Edge Outputs	1.066GHz x 40 Edges 4.266GHz x 10 Edges (when multiplexed)
Delay Resolution	1.83ps
INL (Integral Non-Linearity)	+/- 3.89ps
Random Jitter	Max. 0.7ps rms
Total Deterministic Jitter	Max. +/- 8.4ps (under maximum interference condition)

Figure 28.6.6: Prototype chip specification.

Continued on Page 670

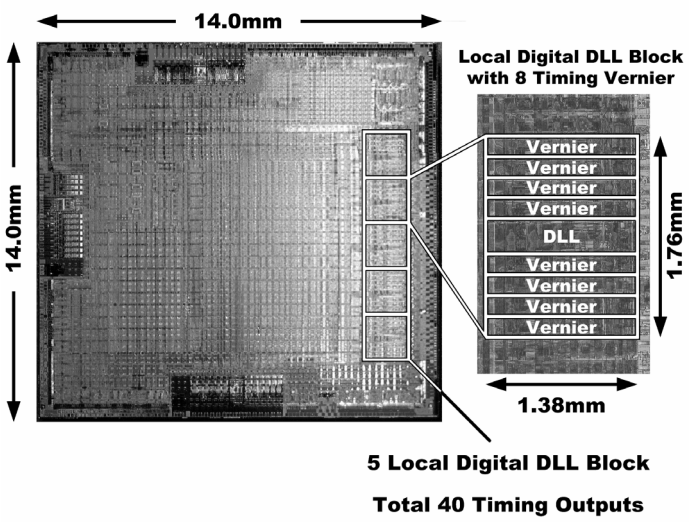

Figure 28.6.7: Die photo and sizes.

